IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
	)	
FAN ET AL.	)	Examiner: HARRISON, MONICA D.
	)	
Serial No.: 10/055,265	)	Art Unit: 2829
	)	
Filed: 01/22/2002	)	Docket No.: JCLA8124
	)	
For: METHOD FOR FABRICATING A NON-VOLATILE MEMORY	)	

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-0710 (order No. JCLA8124).

RESPONSE TO OFFICE ACTION

MP Non Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Office Action mailed August 07, 2003 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AMENDMENTS

1. (Currently Amended) A method for fabricating a non-volatile memory, comprising:

providing a substrate having a strip stacked structure thereon, wherein the strip stacked structure comprises a gate conductive layer and a dielectric layer under the gate conductive layer;

forming a buried drain line as a buried bit line in the substrate beside the strip stacked structure;

forming an insulating layer on the buried drain line;

forming sequentially a silicon layer and a cap layer over the substrate covering the strip stacked structure and the insulating layer;

patterning the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line to form a ~~plurality of~~ stacked gate structure~~s~~, wherein the patterned silicon layer serves as a word line;

forming a liner layer on exposed surfaces of the silicon layer, the gate structures and the substrate;

removing the cap layer; and

forming a metal salicide (self-aligned silicide) layer on the silicon layer.

2. (Currently Amended) A method for fabricating a nitride read-only memory (NROM), comprising:

providing a substrate having a strip stacked structure thereon, wherein the strip stacked structure comprises a gate conductive layer and a charge trapping layer under the gate conductive layer;

forming a buried drain line as a buried bit line in the substrate beside the strip stacked structure;

forming an insulating layer on the buried drain line;

forming sequentially a silicon layer and a cap layer over the substrate covering the strip stacked structure and the insulating layer;

patterning the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line to form a ~~plurality of~~ stacked gate structure~~s~~, wherein the patterned silicon layer serves as a word line;

forming a liner layer on exposed surfaces of the silicon layer, the gate structures and the substrate;

removing the cap layer; and

forming a metal salicide (self-aligned silicide) layer on the silicon layer.

3. (Original) The method of claim 2, wherein forming the metal salicide layer comprises forming a titanium salicide layer.

4. (Original) The method of claim 3, wherein forming the titanium salicide layer requires a temperature from about 600°C to about 800°C.

5. (Original) The method of claim 2, wherein forming the metal salicide layer comprises forming a cobalt salicide layer.

6. (Original) The method of claim 5, wherein forming the cobalt salicide layer requires a temperature from about 600°C to about 700°C.

7. (Original) The method of claim 2, wherein the charge trapping layer comprises one selected from the group consisting of a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer, a silicon nitride/silicon nitride/silicon nitride (NNN) stacked layer and a silicon nitride/silicon nitride/silicon oxide (NNO) stacked layer.

8. (Original) The method of claim 2, wherein the liner layer comprises silicon oxide.

9. (Original) The method of claim 2, wherein the silicon layer comprises polysilicon.

10. (Original) The method of claim 2, wherein the insulating layer comprises silicon oxide formed from tetraethyl-ortho-silicate (TEOS-oxide).

11. (Original) The method of claim 2, wherein the cap layer comprises silicon nitride.

12. (Currently Amended) A method for fabricating a read-only memory, comprising:

providing a substrate having a strip stacked structure thereon, wherein the strip stacked structure comprises a gate conductive layer and a gate dielectric layer under the gate conductive layer;

forming a buried drain line as a buried bit line in the substrate beside the strip stacked structure;

forming an insulating layer on the buried drain line;

forming sequentially a silicon layer and a cap layer over the substrate covering the strip stacked structure and the insulating layer;

patterning the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line to form a ~~plurality of~~ stacked gate structure~~s~~, wherein the patterned silicon layer serves as a word line;

forming a liner layer on exposed surfaces of the silicon layer, the gate structures and the substrate;

removing the cap layer; and

forming a metal salicide (self-aligned silicide) layer on the silicon layer.

13. (Original) The method of claim 12, wherein forming the metal salicide layer comprises forming a titanium salicide layer.

14. (Original) The method of claim 13, wherein forming the titanium salicide layer requires a temperature from about 600°C to about 800°C.

15. (Original) The method of claim 12, wherein forming the metal salicide layer comprises forming a cobalt salicide layer.

16. (Original) The method of claim 15, wherein forming the cobalt salicide layer requires a temperature from about 600°C to about 700°C.

17. (Original) The method of claim 12, wherein the liner layer comprises silicon oxide.

18. (Original) The method of claim 12, wherein the silicon layer comprises polysilicon.

19. (Original) The method of claim 12, wherein the insulating layer comprises silicon oxide formed from tetraethyl-ortho-silicate (TEOS-oxide).

20. (Original) The method of claim 12, wherein the cap layer comprises silicon nitride.